28 V LOW THERMAL IMPEDANCE HBT WITH 20 W CW OUTPUT POWER

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ABSTRACT

AlGaAs/GaAs heterojunction bipolar transistors have been fabricated which exhibit record output power for GaAs flip-chip technology, and record operating voltage for GaAs microwave power devices. Transistors with 2 mm emitter length readily achieve 20 W CW output power at 2 GHz when biased at 28 V, with typical power-added efficiencies of 62% (typical collector efficiencies of 70%). Maximum CW output power of 25 W has been obtained, corresponding to a power density of 12.5 W/mm.

INTRODUCTION

GaAs heterojunction bipolar transistor (HBT) technology has the potential for providing drop-in replacements for existing silicon bipolar power transistors, delivering much higher power gain and up to twice the RF output power for a given amount of DC power. Such components, if available, would find application in systems where the performance of silicon bipolar transistors is inadequate, such as solid-state transmitters for air traffic control and other radar systems, and efficient, linear power amplifiers.

Historically, three obstacles have prevented widespread implementation of such GaAs HBT replacements: high cost, relatively low power levels (usually <10 W), and relatively low operating voltages (usually <10 V).

The first two obstacles — cost and low power — are both due in part to the low thermal conductivity of GaAs. The fact that the thermal conductivity of GaAs is only about 1/3 that of silicon clearly places a constraint on the maximum power which can be dissipated for a given die size. Conventional GaAs power devices must necessarily be relatively large in order to maintain acceptable junction temperatures. Larger size also translates to increased expense, since chip cost is proportional to die size.

The third obstacle — low operating voltage — is not fundamental, but rather historical in nature. The development of HBT technology has been driven by low-voltage, low-power wireless communications applications below 5 GHz, and by military applications at higher frequencies. Because of the fundamental tradeoffs involved, HBTs designed for higher frequencies have also used relatively low operating voltages, typically 10 V or less. However, GaAs HBTs are capable of efficient operation at higher voltages, as we recently demonstrated [1].

In this paper we report results for an HBT technology which simultaneously addresses the issues of thermal resistance, die size, and operating voltage. By applying Low Thermal Impedance (LTI) technology [2] to HBT structures designed specifically for L/S-band operation, we obtain high-voltage devices with very small die sizes, with thermal resistance dominated by metallization rather than by semiconductor. These devices demonstrate for the first time the feasibility of GaAs HBTs for high-performance drop-in replacements for silicon bipolar power transistors.

DEVICE FABRICATION

The HBT epitaxial structure shown in Table I was grown on semi-insulating GaAs by metal-organic chemical vapor deposition. The 2.8 μm thick collector layer provides a base-collector breakdown voltage BV_{CBO} of 70 V.

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Table I. Epitaxial structure of 28 V HBT.

Layer	Material	Thickness (nm)	Doping (cm^{-3})
Contact cap	$In_{0.5}Ga_{0.5}As$	30	Si: 1 x 10^{19}
Grading	InGaAs-GaAs	30	Si: 1 x 10^{19}
Emitter cap	GaAs	190	Si: 5 x 10^{18}
Grading	GaAs-AlGaAs	50	Si: 3 x 10^{17}
Emitter	$Al_{0.35}Ga_{0.65}As$	60	Si: 3 x 10^{17}
Grading	AlGaAs-GaAs	20	Si: 3 x 10^{17}
Base	GaAs	800	C: 4 x 10^{19}
Collector	GaAs	2800	Si: 6 x 10^{15}
Subcollector	GaAs	500	Si: 5 x 10^{18}
Buffer	$Al_{0.4}Ga_{0.6}As$	100	Undoped

Basic fabrication (device isolation, formation of ohmic contacts, capacitors, and resistors) was accomplished using a process similar to TI's production HBT process [3]. An emitter stripe width of 4 μm, together with non-self-aligned base contacts and a depleted emitter ledge structure for surface passivation, were used to obtain high yield and reliable operation. The devices were designed to be unconditionally thermally stable by means of base ballast networks, which have less impact on efficiency than the emitter ballast used by silicon bipolar transistors [4].

After basic device fabrication was completed, the LTI process was used for the remaining frontside and backside process steps, as described in the following. Au was plated to a thickness of 3 μm to build up the transmission lines and to form airbridges to the emitters. This plated metal also covered most of the wafer surface to provide a microwave groundplane. Non-grounded components (such as base and collector leads) were then covered by a 10 μm thick polyimide layer. A second plating step was performed to increase the plated Au thickness to 10 μm. The final processing step on the front side of the wafer was sputter deposition of Au to cover the polyimide, providing a low-loss groundplane for the transmission lines embedded in the polyimide. The wafers were then mechanically thinned and polished to achieve a thickness of 100 μm with a specular backside surface suitable for photolithography. After wafer thinning, through-wafer vias were etched and backside plating was performed to obtain electrical connections to the frontside of the wafer.

For clarity, the side of the chip which contains the transistors is referred to as the "active side," while the other side is referred to as the "passive side." The chip is assembled with the active side against the heat sink for efficient heat removal. Because connections for DC power and RF input/output are made on the passive side of the chip, the flip-chip nature of the die is not detectable without a microscope; no special alignment or flip-chip packaging or assembly is required. In fact, LTI transistors and MMICs can be designed to provide die which are exact drop-in replacements of die for existing conventional components — except that the LTI components provide higher power densities with lower junction temperatures.

RF TESTING

Completed die were mounted on either copper or copper-molybdenum carriers with AuSn solder; no significant differences were seen between devices mounted on copper or copper-molybdenum. Transistors with 2 mm total emitter length were tested at 2 GHz, with external tuning on the input and output to achieve a match to 50 Ω. The output of the device under test was monitored with a spectrum analyzer at all times to insure that no oscillations were present. No tuner or fixture losses were de-embedded, and no intentional harmonic tuning was applied.

The results presented in this paper were obtained with a common-emitter transistor design consisting of 20 emitter fingers in parallel, spaced 40 μm apart; each emitter finger is $4 \times 100\ \mu m^2$. The total area required for the transistor, including base ballast network and through-chip vias for contacting the base and collector from the passive side of the chip, is roughly $0.8 \times 0.8\ mm^2$, or less than 12% of the chip size required for the conventional 30 W HBT we reported previously [1]. The active and passive sides of the chip are shown in Figures 1 and 2, respectively. More than ten devices from two different epitaxial growth runs have been tested to 20 W at a collector bias of 28 V, with typical associated power-added efficiency of 62% (typical collector efficiency of 70%). The highest power-added efficiency measured at 20 W CW output power at 2 GHz was 64.4% PAE (70.7% collector efficiency) with 11.1 dB associated gain under class-B operation (zero quiescent current). This was achieved at 28 V, with 1.01 A collector current. The

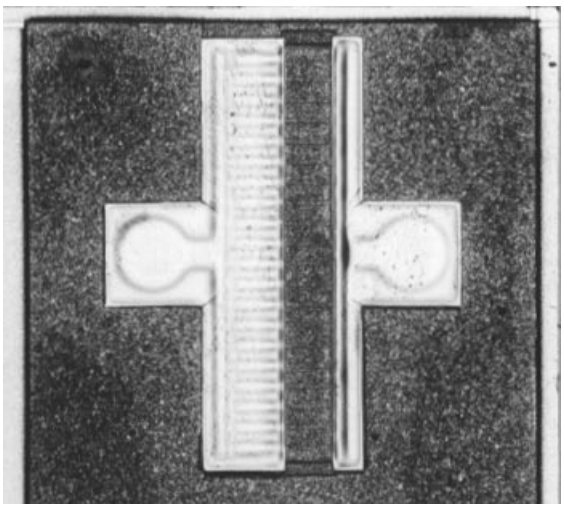

Figure 1. Active side of 20 W HBT

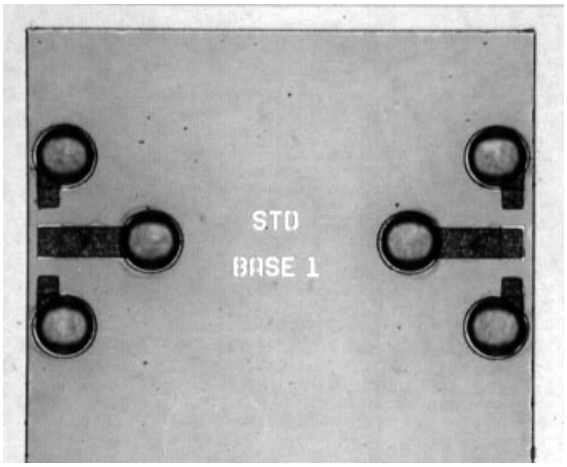

Figure 2. Passive side of 20 W HBT

maximum junction temperature rise was 100° C above baseplate at this power dissipation, as predicted by thermal modeling and confirmed by IR scan. When tuned for maximum gain under class-B operation, power gain of 15 dB was obtained (power gain under linear class-A operation was not measured, but would be expected to be several dB higher).

Despite the high power density, these devices are not particularly sensitive to variations in baseplate temperature. As shown in Figure 3, CW output power dropped only 0.3 dB from 15.8 W (42 dBm) at 0° C to 14.8 W (41.7 dBm) at 60° C baseplate temperature, while power-added efficiency dropped from 64% to 61.7% (collector efficiency from 71.4% to 69.4%).

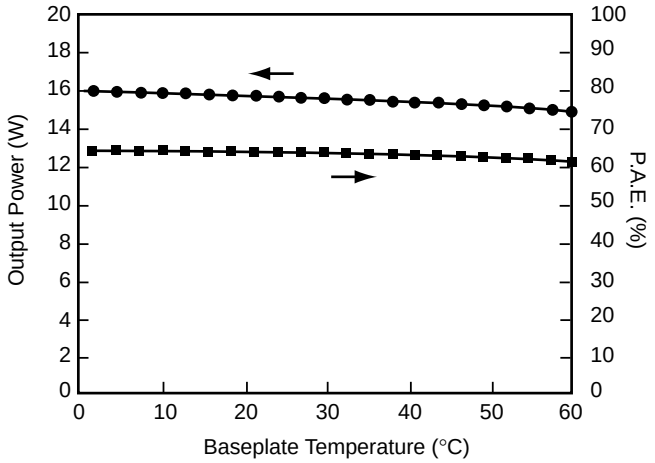

Figure 3. Output power and power-added efficiency vs. baseplate temperature

DISCUSSION

To our knowledge, the results presented in this paper represent state-of-the-art performance for CW power transistors in this frequency range, despite the fact that they were obtained with a first-pass unit cell design. Improvements to the cell design, the use of harmonic tuning, and pulsed operation may result in substantially higher efficiency and peak output power. However, even without such changes, the power gain is sufficiently high that straightforward power-combining of these compact cells should result in single-chip power levels which are unprecedented for GaAs microwave devices.

Although 20 W operation corresponds to a high power density of 10 W/mm, the record operating voltage and wide emitter stripe allowed for a relatively low emitter current density of 12.6 kA/cm^2. Low current density is important for long-term reliability, since HBT median time to failure is inversely proportional to the square of current density [5-6]. Because thermal resistance is dominated by metallization (temperature drop across semiconductor accounts for only 25% of the total thermal resistance according to simulations), the maximum junction temperature rise of 100° C is relatively low compared to many commercially-available power transistors. For applications where even lower junction temperature is required, these devices may be operated at reduced power levels of 10 to 15 W with no degradation of power gain or efficiency. Finally, it should be noted that 20 W at 28 V represents a nominal operating point only; transistors of this design have been operated to 25 W CW output power, and bias levels up to 31.5 V.

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The per-wafer cost of LTI technology is somewhat higher than for standard HBTs because of additional processing steps. Nevertheless, the cost per Watt may ultimately be lower than for other GaAs technologies because of LTI's higher power density. Compared to 5.3 W/mm^2 (*saturated* output power per unit area of GaAs die) for a high-performance power FET [7], the demonstrated *nominal* power density of >31 W/mm^2 gives the LTI technology a considerable advantage in die size.

CONCLUSION

HBTs fabricated using Low Thermal Impedance technology have demonstrated record operating voltage for GaAs microwave devices, and state-of-the-art performance for CW power transistors at S-band. At 2 GHz, a common-emitter HBT biased at 28 V delivered 20 W CW output power with 11.1 dB gain and 64.4% power-added efficiency (collector efficiency of 70.7%) under class-B operation. Despite use of a very compact device occupying roughly 0.8×0.8 mm^2, the maximum junction temperature rise was only 100° C above baseplate. The ability to fabricate high-performance GaAs HBTs with operating voltages compatible with existing silicon bipolar power devices should allow relatively straightforward upgrades of existing systems. The demonstrated power/efficiency performance should also be attractive for emerging applications with stringent requirements on volume and cooling, such as compact base stations for wireless communications.

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